A Micropower, 2-channel, 187.5-ksps, Serial-Output 12-bit SAR ADC

FEATURES

- Pin-for-pin, 1.5x Faster Upgrade to AD7887
- Single-supply Operation: +2.7V to +3.6V
- INL: ±1LSB
- One or Two Single-ended Analog Inputs
- Internal Wide-bandwidth Track-and-Hold
- Integrated +2.5-V Reference
- Flexible Power/Throughput-Rate Management
  - 0.85mA at 187.5ksps (Internal VREF ON)
  - 0.7mA at 187.5ksps (Internal VREF OFF)
- Shutdown-mode Supply Current: 1µA (max)
- SPI®/QSPI™/MICROWIRE™/DSP-Compatible Serial Interfaces[1]
- Operating Temperature Range: -40ºC to +85ºC
- 8-pin MSOP Packaging

APPLICATIONS

Instrumentation and Control Systems
High-Speed Modems
Battery-powered systems:
Personal Digital Assistants, Medical Instruments, Mobile Communications

DESCRIPTION

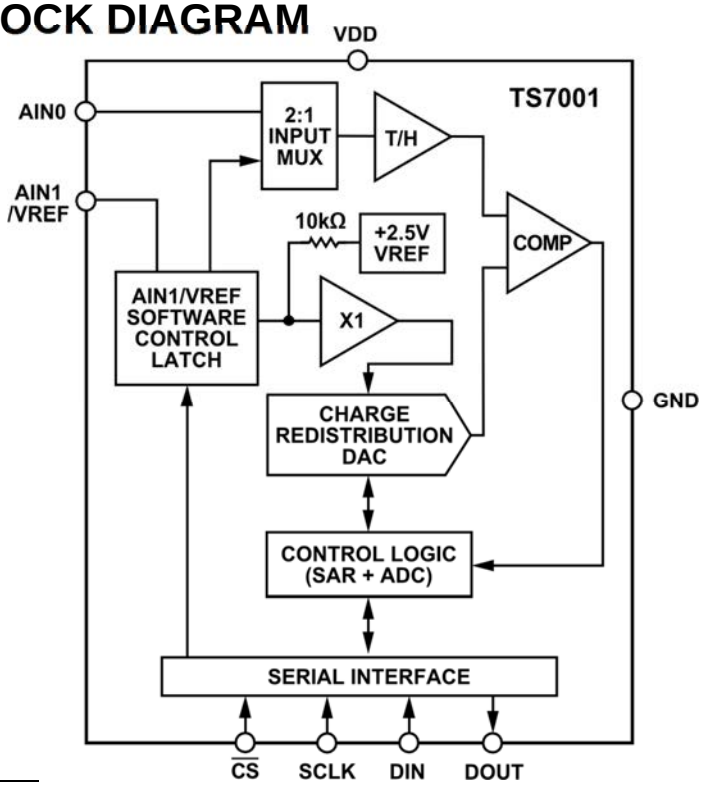
The TS7001 – a pin-for-pin, 1.5x faster alternate to the AD7887 - is a self-contained, 2-channel, high-speed, micropower, 12-bit analog-to-digital converter (ADC) that operates from a single +2.7V to +3.6V power supply. The TS7001 is capable of a 187.5-ksps throughput rate with an external 3 MHz serial clock and draws 0.85mA supply current.

The wideband input track-and-hold acquires signals in 500ns and features a single-ended sampling topology. Output data coding is straight binary and the ADC is capable of converting full power signals up to 10 MHz. The ADC also contains an integrated 2.5V reference or the VREF pin can be overdriven by an external reference.

The TS7001's provides one or two analog inputs each with an analog input range from 0 to V_{REF}. In two-channel operation, the analog input range is 0V to VDD. Efficient circuit design ensures low power consumption of 2mW (typical) for normal operation and 3µW in power-down operation.

The TS7001 is fully specified from -40ºC to +85ºC and is available in 8-pin MSOP package.

FUNCTIONAL BLOCK DIAGRAM



[1] SPI and QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corporation

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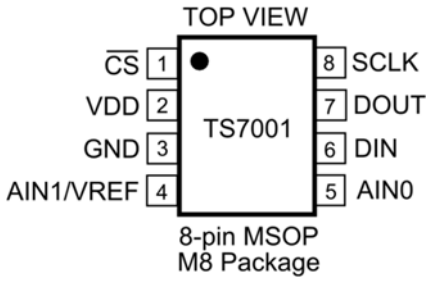
ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... −0.3V to +7V
Analog Input Voltage (AIN0, AIN1) to AGND .... −0.3V to V_{DD} + 0.3V
Digital Input Voltage to AGND..... −0.3V to V_{DD} + 0.3V
Digital Output Voltage to AGND..... −0.3V to V_{DD} + 0.3V
REFIN/REFOUT to AGND ..... −0.3V to V_{DD} + 0.3V
Input Current to Any Pin Except Supplies[1].....±10mA
Operating Temperature Range .....−40°C to +125°C
Storage Temperature Range .....−65°C to +150°C
Junction Temperature .....+150°C

MSOP Package Power Dissipation 450mW
θ_{JA} Thermal Impedance.....205.9°C/W
θ_{JC} Thermal Impedance.....43.74°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec)..... 215°C
Infrared (15 sec) ..... 220°C
Pb-Free Temperature, Soldering Reflow.....260(0)°C
ESD 4kV

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS7001IM8	TADF	Tube	50
TS7001IM8T		Tape & Reel	2500

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +3.6V; V_{REF} = 2.5V External/internal reference unless otherwise noted; f_{SCLK} = 3 MHz;
$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Limit[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal to Noise + Distortion Ratio (SNR)[2]	71	dB (typ)	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 187.5ksps
Total Harmonic Distortion (THD)	−80	dB (typ)	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 187.5ksps
Peak Harmonic or Spurious Noise	−80	db (typ)	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 187.5ksps
Intermodulation Distortion (IMD)			
Second-Order Terms	−80	dB (typ)	f1 = 9.983 kHz, f2 = 10.05 kHz, f_{SAMPLE} = 187.5ksps
Third-Order Terms	−80	dB (typ)	f1 = 9.983 kHz, f2 = 10.05 kHz, f_{SAMPLE} = 187.5ksps
Channel-to-Channel Isolation	−80	dB (typ)	f_{IN} = 25 kHz
Full-Power Bandwidth	10	MHz (typ)	Measured at 3 dB down
DC ACCURACY(Any channel)			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB (max)	VDD = 3V
Differential Nonlinearity	±1	LSB (max)	VDD = 3V; Guaranteed no missing codes to 11 bits
Offset Error	±4	LSB (max)	VDD = 3V, dual-channel mode
	±6	LSB (typ)	Single-channel mode
Offset Error Match	0.5	LSB (max)	
Gain Error	±2	LSB (typ)	Dual-channel mode
	±1	LSB (max)	Single-channel mode, external reference
	±6	LSB (typ)	Single-channel mode, internal reference
Gain Error Match	2	LSB (max)	
ANALOG INPUT			
Input Voltage Range	0 to VREF	V	Single-channel operation
	0 to VDD	V	Dual-channel operation
Leakage Current	±5	µA (max)	
Input Capacitance	10	pF (typ)	
REFERENCE INPUT/OUTPUT			
REFIN Input Voltage Range	2.5/VDD	V (min/max)	Single-channel/Dual-channel; Functional from 1.2V
Input Impedance	10	kΩ (typ)	Very high impedance if internal reference is disabled
REFOUT Output Voltage	2.488/2.513	V (min/max)	Initial accuracy = 0.5%
REFOUT Temperature Coefficient	30	ppm/°C (typ)	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.1	V (min)	VDD = 2.7V to 3.6V
Input Low Voltage, V_{INL}	0.8	V (max)	VDD = 2.7V to 3.6V
Input Current, I_{IN}	±1	µA (max)	Typically 10nA, V_{IN} = 0V or VDD
Input Capacitance, C_{IN}[3]	10	pF (max)	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.5	V (min)	V_{DD} = 2.7V to 3.6V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V (max)	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA (max)	
Floating-State Output Capacitance[4]	10	pF (max)	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Throughput Time	16	SCLK cycles	Conversion time plus acquisition time is 187.5ksps, with 3 MHz Clock
Track-and-Hold Acquisition Time	1.5	SCLK cycles	
Conversion Time	14.5	SCLK cycles	4.833 µs (3 MHz Clock)

ELECTRICAL SPECIFICATIONS (continued)

V_{DD} = +2.7V to +3.6V; V_{REF} = 2.5V External/internal reference unless otherwise noted; f_{SCLK} = 3 MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Limit[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
VDD	+2.7/+3.6	V (min/max)	
IDD			
Normal Mode[4] (PM Mode 2)			
Static	0.6	mA (max)	
Operational (f_{SAMPLE} = 187.5 ksps)	0.85	mA (typ)	Internal reference enabled
	0.7	mA (typ)	Internal reference disabled
Using Standby Mode (PM Mode 4)	0.45	mA (typ)	f_{SAMPLE} = 50 ksps
Using Shutdown Mode (PM Modes 1 and 3)	0.12	mA (typ)	f_{SAMPLE} = 10 ksps
	0.012	mA (typ)	f_{SAMPLE} = 1 ksps
Standby Mode[5]	0.21	mA (max)	VDD = 2.7V to 3.6V
Shutdown Mode[5]	1	µA (max)	VDD = 2.7V to 3.6V
Normal Mode Power Dissipation	2.1	mW (max)	VDD = 3 V
Shutdown Power Dissipation	3	µW (max)	VDD = 3 V
Standby Power Dissipation	0.63	mW (max)	VDD = 3 V

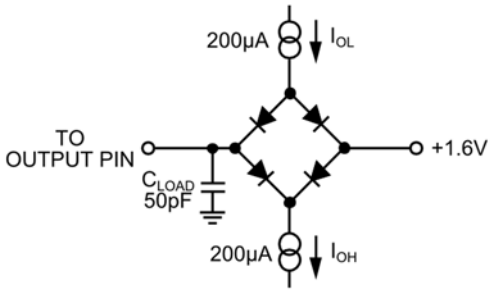
Note 1: The TS7001's temperature range is –40°C to +85°C.
Note 2: SNR calculation includes distortion and noise components.
Note 3: Sample tested at T_A = 25°C to ensure compliance.
Note 4: All digital inputs at GND except for $\overline{CS}$ at V_{DD}. All digital outputs are unloaded. Analog inputs are connected to GND.
Note 5: SCLK is at GND when SCLK is off. All digital inputs are at GND except for $\overline{CS}$ at VDD. All digital outputs are unloaded. Analog inputs are connected to GND.

TIMING SPECIFICATIONS[1]

V_{DD} = +2.7V to +3.6V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Limit	Unit	Description
f_{SCLK}[2]	3	MHz (max)	External serial clock
$t_{CONVERT}$	14.5 × t_{SCLK}		Conversion Time
t_{ACQ}	1.5 × t_{SCLK}		Throughput Time = $t_{CONVERT}$ + t_{ACQ} = 16 t_{SCLK}
t_1	10	ns (min)	$\overline{CS}$ to SCLK Setup Time
t_2[3]	60	ns (max)	Delay from $\overline{CS}$ until DOUT three-state disabled
t_3[3]	100	ns (max)	Data Access Time after SCLK High-to-Low Edge
t_4	20	ns (min)	Data Setup Time prior to SCLK Low-to-High Edge
t_5	20	ns (min)	Data Valid to SCLK Hold Time
t_6	0.4 × t_{SCLK}	ns (min)	SCLK high Pulse Width
t_7	0.4 × t_{SCLK}	ns (min)	SCLK low Pulse Width
t_8[4]	80	ns (max)	$\overline{CS}$ rising edge to DOUT High-Z
t_9	5	µs (typ)	Power-up Time from Shutdown

Note 1: Timing specifications are sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of VDD) and timed relative to a voltage level of 1.6V.
Note 2: The mark/space ratio for the SCLK input is 40/60 to 60/40. See Serial Interface section for additional details.
Note 3: Measured with the load circuit as shown below and defined as the time required for the output to cross 0.8V or 2.0V.
Note 4: Timing specification t_8 is derived from the measured time taken by the data outputs to change 0.5V when loaded with the circuit shown below. The measured result is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the TS7001 and is independent of bus loading.

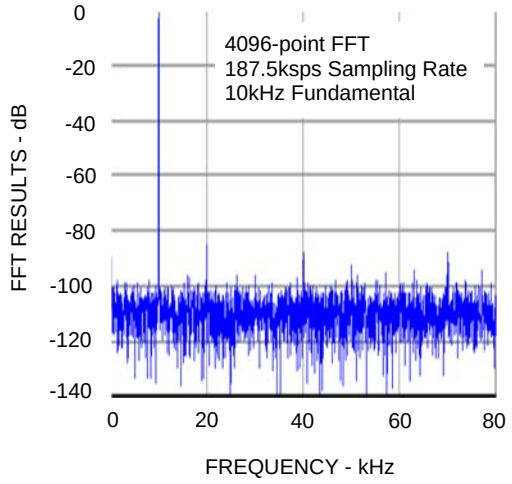


Load Circuit Used for TS7001's Digital Output Timing Specifications.

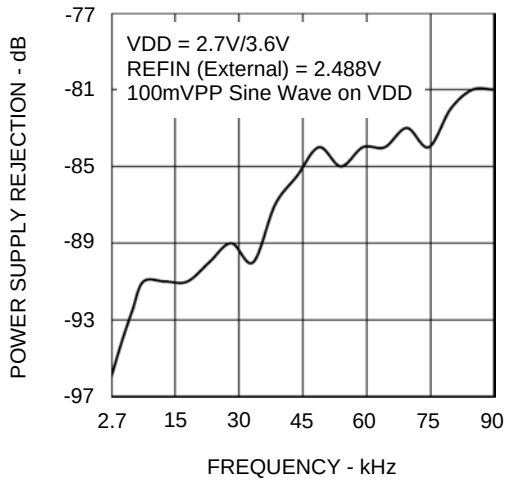
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = +3V; f_{SCLK} = 3MHz; T_A = 25ºC, unless otherwise noted.

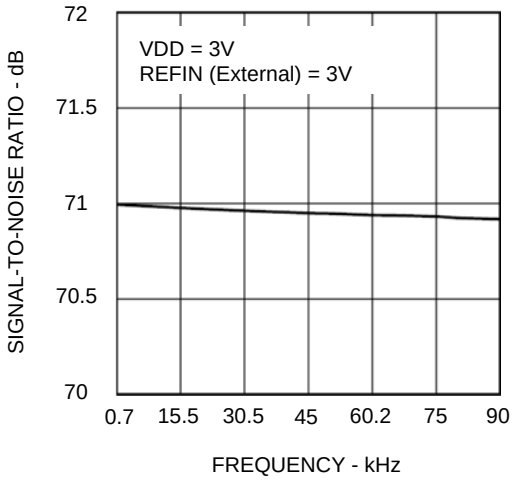
Dynamic Performance vs Frequency



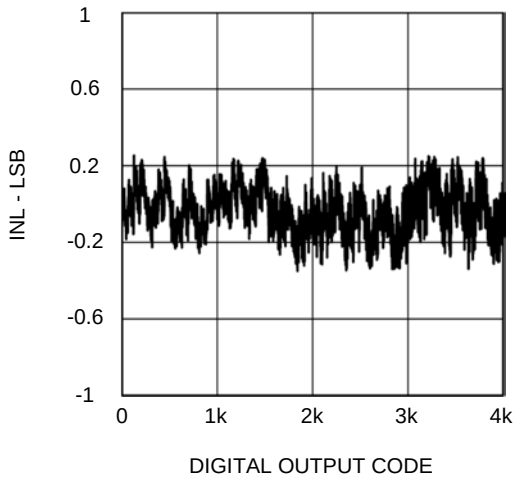
Power Supply Rejection vs Frequency



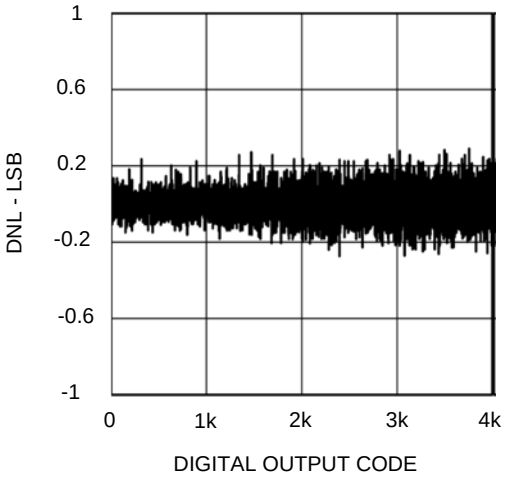
Signal-to-Noise Ratio vs Frequency



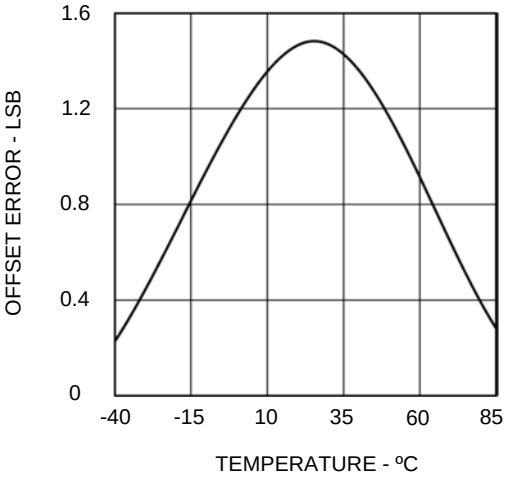
Integral Nonlinearity



Differential Nonlinearity



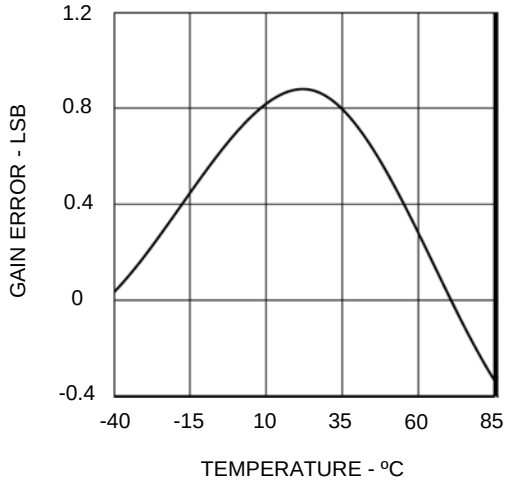
Offset Error vs Temperature



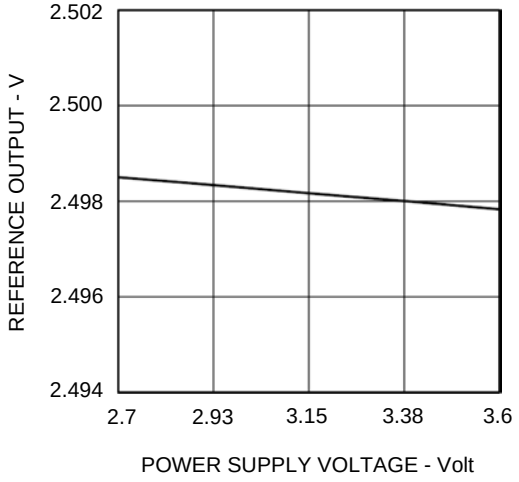
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = +3V; f_{SCLK} = 3MHz; T_A = 25ºC, unless otherwise noted.

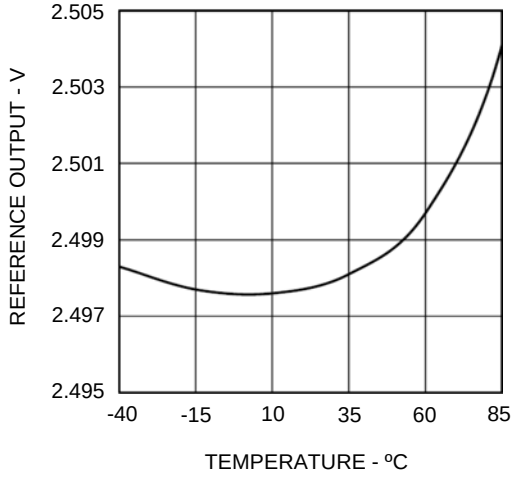
Gain Error vs Temperature



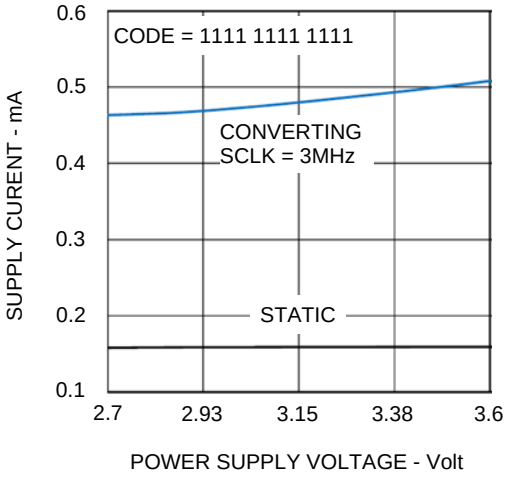
Internal Reference Output vs Supply Voltage



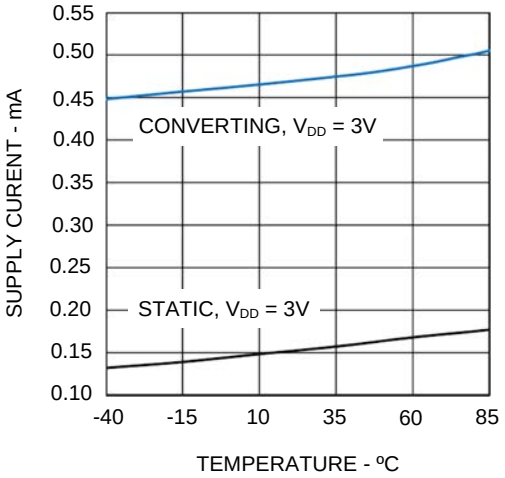
Internal Reference Output vs Temperature



Power Supply Current vs Power Supply Voltage



Power Supply Current vs Temperature



PIN FUNCTIONS

PIN	LABEL	DESCRIPTION
1	$\overline{CS}$	Chip Select: As an active low logic input signal, the $\overline{CS}$ input provides the dual function of initiating TS7001 conversions as well as framing the serial data transfer. When the TS7001 is operated in Mode 1(its default power management mode), the $\overline{CS}$ pin also acts as the shutdown pin in that the TS7001 is powered-down when the $\overline{CS}$ pin is logic high.
2	VDD	Power Supply Voltage: The TS7001's V_{DD} range +2.7V to +3.6V. In two-channel operation, the VDD pin also serves as the TS7001's voltage reference source during conversions. For optimal performance, the VDD pin should be bypassed to GND with a 10-µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor.
3	GND	Analog Ground Pin: The GND pin is the ground reference point for all TS7001 internal circuitry. In systems with separate AGND and DGND planes, the TS7001's GND pin should be connected to the AGND plane.
4	AIN1/VREF	Analog Input Channel 1/External VREF Input: In single-channel mode, the AIN1/VREF pin is configured as VREFIN/OUT. In this mode, the TS7001's internal 2.5V reference can be accessed or an external reference can be applied to this pin thereby overriding the internal reference. The reference voltage range for an externally-applied reference is 1.2V to VDD. In two-channel mode, the AIN1/VREF pin operates as a second analog input channel, AIN1. The input voltage range on AIN1 is 0 to VDD.
5	AIN0	Analog Input Channel 0: In single-channel operation, AIN0 is the TS7001's analog input with an input voltage range of 0V to VREF. In two-channel operation, the AIN0 pin exhibits an analog input range of 0V to VDD.
6	DIN	Serial Data Input: Serial data to be loaded into the TS7001's control register is applied at the DIN pin. Serial data is loaded into the ADC from the host processor on low-to-high SCLK transitions (see the Control Register section for additional information). Configuring the TS7001 as a single-channel, read-only ADC can be achieved by hard-wiring the DIN pin to GND or by applying a logic LOW at all times at the DIN pin.
7	DOUT	Serial Data Output: The TS7001's conversion result is available on this pin. Serial data is transferred out of the TS7887 on high-to low transitions of SCLK. The 12-bit conversion result is comprised of four leading zeros followed by the 12 bits of conversion data formatted MSB first. Thus, a total of 16 SCLK high-to-low transitions transfers the conversion result to the host processor as shown in the corresponding timing diagram of Figure 14.
8	SCLK	Serial-Clock Input: SCLK is used for (3) purposes: a) to load serial data from the host processor into the TS7001's control register on low-to-high SCLK transitions; b) to transfer the 12-bit conversion result to the host processor on high-to-low SCLK transitions; and c) to control the TS7001's conversion process.

TS7001 CONTROL REGISTER DESCRIPTION

The TS7001's write-only control register is 8-bits wide. Serial ADC configuration data is uploaded from the host processor at the TS7001's DIN pin on low-to-high SCLK transitions. Serial input data is uploaded to the TS7001 simultaneously as the conversion result is transferred out of the TS7001. All serial data transfers require 16 serial clocks transitions. After a high-to-low $\overline{CS}$ transition signal, serial data available on the first eight low-to-high SCLK transitions is transferred into the control register. The first bit in the serial data stream is always interpreted as the MSB. Upon initial power-up, the TS7001's default control register bit is cleared to all zeros (all "0"s). Table 1 lists the functions of the Control Register's 8 bits.

Table 1. TS7001's 8-Bit Control Register Content Description

DB7 (MSB)	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
DONTC	ZERO	REF	SIN/DUAL	CH	ZERO	PM1	PM0

DBx	Label	Comment
7	DONTC	Control Register DB7: Bit status of DB7 is "Don't Care." In other words, the DB7 bit can be a "0" or a "1".
6	ZERO	Control Register DB6: To ensure correct TS7887 operation, Control Register DB6 status must always be a "zero" ("0").
5	REF	Control Register DB5 – Internal Voltage Reference Configuration: The status of DB5 determines whether the TS7001's internal voltage reference is enabled or disabled. A "0" in the DB5 location will enable the TS7001's internal voltage reference (default condition). To disable the TS7001's internal voltage reference, a "1" must be written into DB5's register location.
4	SIN/DUAL	Control Register DB4 - Single-Channel/Dual-Channel Configuration. Control Register DB4 configures the TS7001 as a single-channel or two-channel ADC. Loading a "zero" ("0") into this register location configures the TS7001 for single-channel operation with the AIN1/VREF pin configured to for internal VREF operation (default configuration). In this case, the analog input signal range is 0V to VREF. Loading a "one" ("1") into this register location configures the TS7001 for two-channel operation with the AIN1/VREF pin configured to its AIN1 function as the second analog input. In addition, the conversion process's reference voltage is internally connected to VDD. In this case, the analog input signal range is 0V to VDD. To obtain best performance from the TS7001 in two-channel operation, the ADC's internal reference should be disabled; that is, a "1" should be loaded into DB5's register location.
3	CH	Control Register DB3 - Channel Select Bit: The bit status of DB3 determines on which channel the TS7001 is converting. When the ADC is configured for dual-channel operation, DB3 determines which channel is converted on the next conversion cycle. When DB3 is a "zero" (a "0"), the AIN0 input is selected and, when DB3 is a "one" (a "1"), the AIN1 input is selected. DB3 should be a "zero" ("0") when the TS7001 is configured for single-channel operation.
2	ZERO	Control Register DB2: To ensure correct TS7887 operation, Control Register DB2 status must always be a "zero" ("0").
1	PM1	Control Register DB1 and DB0 - Power Management Operating Modes: DB1 and DB0 are decoded to configure the TS7001 into one of four operating modes as shown in Table 2.
0	PM0	

Table 2. TS7001's Power Management Operating Modes

PM1	PM0	Mode
0	0	**PM Mode 1:** In this operating mode, the TS7001's power-down mode is enabled if its $\overline{CS}$ input is a "one" (a "1") and is operating in full-power mode when its $\overline{CS}$ input is a "zero" (a "0"). Thus, the TS7001 is powered down on a low-to-high $\overline{CS}$ transition and is powered up on a high-to-low $\overline{CS}$ transition.
0	1	**PM Mode 2:** In this operating mode and regardless of the status of any of the logic inputs, the TS7001 is always fully powered up.
1	0	**PM Mode 3:** In this operating mode, the TS7001 is automatically powered down at the end of each conversion regardless of the state of the $\overline{CS}$ input. ADC wake-up time from full shutdown is 5µs and system design should ensure that at least 5µs have elapsed before attempting to perform a conversion in this mode; otherwise, an invalid conversion result may occur.
1	1	**PM Mode 4:** In this operating mode, the TS7001 is configured for standby operation after conversion. Sections of the TS7001 are powered down; however, the internal 2.5-V reference voltage remains powered up. While PM Mode 4 is similar to PM Mode 3, PM Mode 4 operation allows the TS7001 to power up much faster. For optimal performance, the Control Register's REF bit (DB5) should be a "zero" ("0") to ensure the internal reference is enabled/remains enabled.

DESCRIPTION OF OPERATION

The TS7001 is a single-supply, low-power, single/dual-channel, 12-bit successive-approximation ADC with an easy-to-use serial interface. The ADC can be operated from a 3V supply (2.7V to 3.6V). When operated from either a 3V, the TS7001 can operate at throughput rates up to 187.5ksps when an external 3 MHz clock is applied.

In a 8-pin MSOP package, the TS7001 integrates a 2.5-V reference, a high-speed track/hold, a successive-approximation ADC, and a serial digital interface. An external serial clock is used to transfer data to/from the ADC and controls the TS7001's conversion process. The TS7001 can be configured for single- or two-channel operation. When configured as a single-channel ADC, the analog input range is 0 to VREF (where an externally applied VREF, if used, can range between 1.2 V and VDD). When the TS7001 is configured for two-channel applications, the analog input range on each channel is set internally from 0V to VDD.

If the TS7001 is configured for single-channel operation, the TS7001 can be operated in a read-only mode by applying a logic LOW at all times to the DIN pin (Pin 6) or by hard-wiring the DIN pin permanently to GND. For maximum flexibility to address multiple configurations based on the application, the DIN input can be used to load ADC configuration data from a host processor into the TS7001's 8-bit Control Register.

TS7001 Operation and Transfer Function

The TS7001 is a successive-approximation ADC, the core of which is a charge-redistribution DAC. Figure 1 illustrates an equivalent circuit for the TS7001 in signal acquisition phase. Here, Switch SW1 is in Position A and Switch SW2 is closed. With the sampling capacitor's terminals connected to the analog input on one side and REF on the other, the analog signal is acquired. During the acquisition phase, the inputs to the comparator are balanced since both inputs are connected to REF.

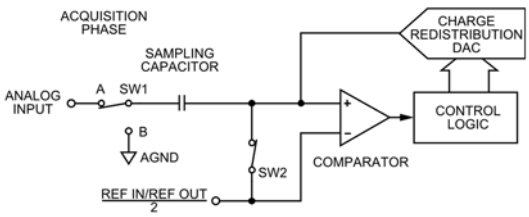


Figure 1:TS7001's Acquisition Phase Equivalent Circuit

During the conversion phase as shown in the equivalent circuit in Figure 2, Switch SW1 is moved from Position A to GND at Position B and Switch SW2 is opened. At this point in time, the inputs to the comparator become unbalanced. The TS7001's control logic and the charge-redistribution DAC work together to add or subtract fixed packets of charge from the sampling capacitor to balance once again the comparator input terminals. At the time when the comparator is rebalanced, the conversion process is complete and the ADC's control logic generates the ADC serial output conversion data.

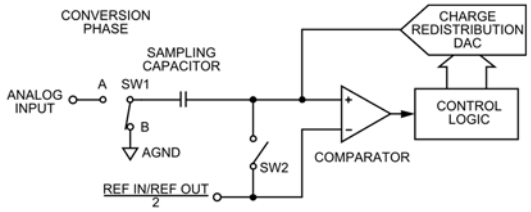


Figure 2: TS7001's Conversion Phase Equivalent Circuit

Figure 3 illustrates the ideal transfer function for the TS7001 where the output data is coded straight binary. Thus, the designed code transitions occur at successive integer LSB values (that is, at 1 LSB, at 2 LSBs, etc) where the LSB size is VREF/4096.

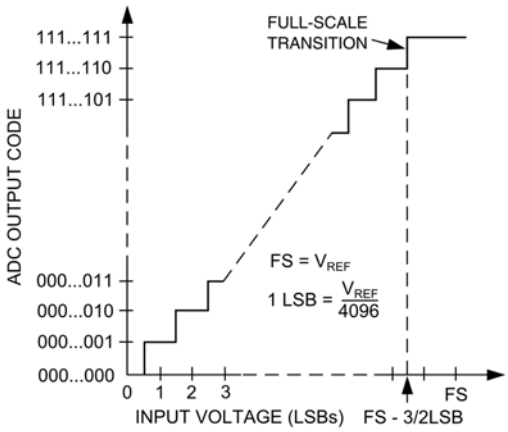


Figure 3: TS7001's Unipolar Transfer Function for Straight Binary Digital Data.

Typical Application Circuit

Figure 4 shows a typical application circuit for the TS7001 where the ADC's GND pin is connected to the analog ground plane of the system. In this application circuit, the TS7001 has been configured for two-channel operation so the ADC's VREF is internally connected to VDD; as a result, the analog input range on either analog input is 0V to VDD. It is always considered good engineering practice to bypass the ADC's VDD with good quality capacitors with short leads (surface-mount components are preferred) and located a very short distance from the ADC. The conversion result at the DOUT pin is a 16-bit word with four leading zeros followed by the MSB of the 12-bit conversion result. In low-power applications, automatic-power-down-at-the-end-of-conversion modes (PM Modes 3 or 4) should be used to improve the ADC's power consumption-versus-throughput rate performance. For additional information on the TS7001's four power management operating modes, please consult the Operating Modes section of the datasheet.

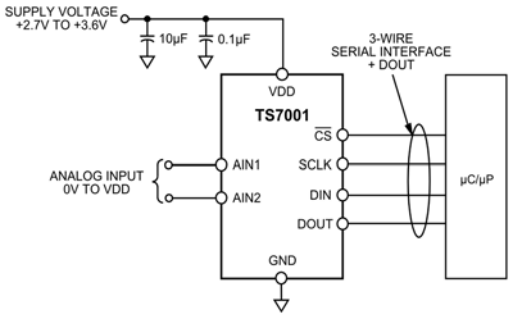


Figure 4: TS7001's Typical Application Circuit.

Analog Input Details

An equivalent circuit of the analog input structure of the TS7001 is illustrated in Figure 5 where diodes D1 and D2 serve as ESD-clamp protection for the analog inputs. Since there are diodes from the analog input to both VDD and GND, it is important any forward conduction of current in D1 or D2 is avoided. Thus, the analog input signal should never exceed the either VDD or GND by more than 200mV. Even though the maximum current these diodes can conduct without causing irreversible damage to the ADC is 20mA, any small amount of forward diode current into the substrate because of an overvoltage condition on an *unselected* channel can cause inaccurate conversion results on the *selected* channel.

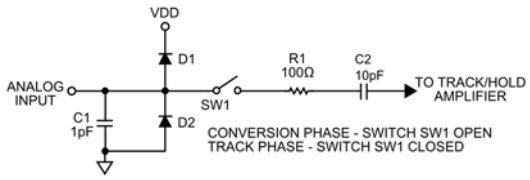


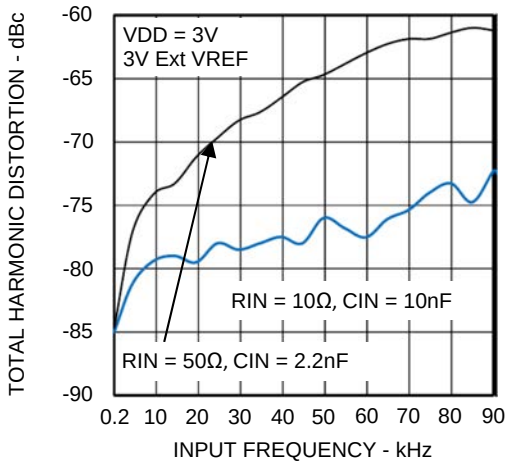
Figure 5: TS7001's Analog Input Equivalent Circuit.

Attributed to parasitic package pin capacitance, capacitor C1 in Figure 5 is typically about 1 pF. Resistor R1 is the equivalent series resistance of the TS7001's input multiplexer and input sampling switch and is approximately 100Ω. Capacitor C2 is the ADC sampling capacitor and has a typical capacitance of 10 pF.

In signal-acquisition (or ac) applications, the use of an external R-C low-pass filter on either or both analog inputs can be useful in removing out-of-band high-frequency components from the analog input signal. In applications where harmonic distortion and signal-to-noise ratio performance are important, the analog input(s) should be driven from a low-impedance source. Large source impedances will affect significantly the TS7001's ac performance. To lower the driving-point impedance level, it may be necessary to use an input buffer amplifier. The optimal choice for the external drive op amp will be determined by application requirements as well as the TS7001's dynamic performance.

When the analog input is not driven by an external amplifier, the driving-point source impedance should be low. The maximum source impedance will depend upon the amount of total harmonic distortion (THD) that can be tolerated in the application. THD will increase as the source impedance increases

Figure 6: TS7001 THD vs Analog Input Frequency



and performance will degrade. Figure 6 illustrates how the TS7001's harmonic performance as a function of frequency is affected by different source impedances.

The TS7001's Internal 2.5-V Reference

Using the REF bit (the DB5 bit) in the TS7001's Control Register, the TS7001's internal 2.5-V reference can be enabled (DB5 cleared to "0") or disabled (DB5 set to "1"). If enabled (the default condition), the internal voltage reference can be used in applications for other purposes and, if this is desired, the reference should be buffered by an external, precision op amp. If an external, precision voltage reference is used instead of the TS7001's internal reference, the internal reference is automatically overdriven. In this case, the TS7001's internal reference should be disabled by setting the REF bit in the control register. When the internal reference is disabled, switch SW1 as shown in Figure 7 opens and the input impedance seen at the AIN1/VREF pin is the reference buffer's input

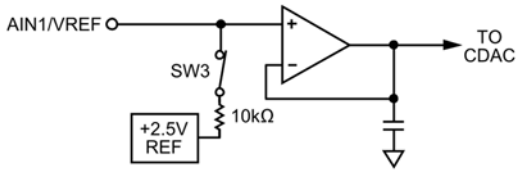


Figure 7: TS7001's Integrated 2.5-V VREF Circuitry.

impedance, approximately in the gigaohm range (GΩ). When the internal reference is enabled, the input impedance at the AIN1/VREF pin is typically 10kΩ. When the TS7001 is configured for two-channel operation, the TS7001's reference is set internally to VDD.

TS7001's Power-Down Operating Modes

The TS7001 provides flexible power management to allow the user to achieve the best power performance for a given throughput rate. The four power management options are selected by programming the TS7001's power management bits ("PM" Bits PM1 and PM0) in the control register as summarized in Table 6. When the PM bits are programmed for either of the auto power-down modes (PM Mode 3 or 4), the TS7001 is powered-down on the 16th low-to-high SCLK transition after a high-to-low $\overline{CS}$ transition. The first high-to-low SCLK transition after a high-to-low $\overline{CS}$ transition powers-up the TS7001 again. When the TS7001 is programmed in PM Mode 1 (i.e., [PM1,PM0] = [0,0], the default condition), the TS7001 is powered down on a low-to-high $\overline{CS}$ transition and powers up from shutdown on a high-to-low $\overline{CS}$ transition. If the $\overline{CS}$ pin is toggled low-to-high during the conversion in this operating mode, the ADC is immediately powered down.

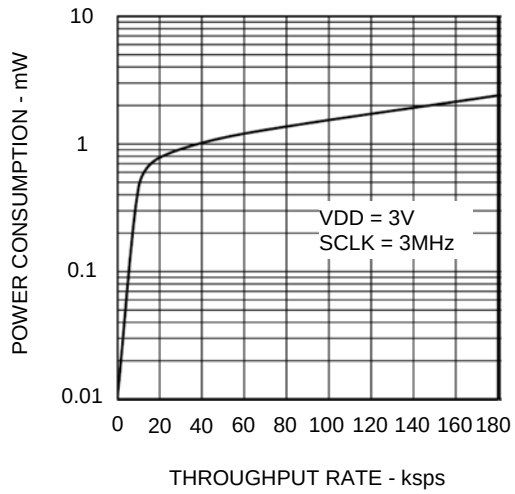
Cold-Start and Standby Power-Up Delay Times

When VDD is first applied to the TS7001 (in other words, from cold start-up), the ADC powers up in PM Mode 1 ([PM1,PM0] = [0,0]). Upon a subsequent high-to-low $\overline{CS}$ transition, the TS7001's power-up delay time is approximately 5µs. When using an external voltage reference in single-channel operation or when the TS7001 is powered up from standby mode (PM Mode 4), its power-up delay time is approximately 1µs because the internal reference has been either disabled (refer to Control Register DB5) or the internal reference has remained powered up (via PM Mode 4). Since the TS7001's power-up delay time PM Mode 4 is very short, powering up the ADC and executing a conversion with valid results in the same read/write operation is feasible.

TS7001 Power Consumption vs. Throughput Rate Considerations

In operating the TS7001 in auto-shutdown mode (PM Mode 3), in auto-standby mode (PM Mode 4), or in PM Mode 1, the average power drawn by the TS7001 decreases at lower throughput rates. As shown in Figure 8, the average power drawn from

Figure 8: TS7001 Power Consumption vs Throughput Rate



the supplies by the ADC is commensurately reduced the longer the TS7001 remains in a powered-down state.

For example, consider the following TS7001 application configuration: (a) the ADC is powered from VDD = 3V and is configured for PM Mode 3 (that is, [PM1, PM0] = [1,0], where the ADC's internal reference is enabled and the ADC automatically powers down after the conversion is completed); and (b) the ADC operates at a throughput rate of 10 ksps with a 3-MHz SCLK.

Given the above configuration, the TS7001's power consumption during normal operation is 2.1mW at VDD = 3 V (0.7mA x 3V). Since its power-up delay time is 5µs and its conversion-plus-acquisition time is ~5.2µs ($t_{CONVERT} + t_{ACQ} = 14.5 \times t_{SCLK} + 1.5 \times t_{SCLK} = 15.5 \times t_{SCLK}$), the TS7001 consumes 3.5mW for 10.2µs during each conversion cycle. Since the conversion cycle time (100µs) is the reciprocal of the ADC's throughput rate (10ksps), the average power consumed by the TS7001 during each conversion cycle is (10.2/100) × (2.1mW), or 214.2µW. The TS7001's power consumption vs. throughput rate when configured for automatic shutdown post conversion and operating on a 3V supply is illustrated in Figure 8.

Power Management Operating Modes

Designed to provide flexible power consumption profiles, the TS7001 incorporates four different operating modes to optimize the ADC's power consumption/throughput-rate ratio. As previously described in Table 6, the four different modes of operation in the TS7001 are controlled by the PM1 and PM0 bits of the Control Register. Also mentioned previously, the TS7001 can be configured as a read-only ADC by forcing an all zeros ("0"s) condition in the control register. This can be easily done by applying a logic LOW at all times to the DIN pin or hard-wiring the DIN pin directly to GND.

Power Management Mode 1 Operation: [PM1,PM0] = [0,0]

Power Management Operating Mode 1 is used to control the TS7001's power-down using the $\overline{CS}$ pin. Whenever the $\overline{CS}$ pin is low, the TS7001 is fully powered up; whenever the $\overline{CS}$ pin is high, the TS7001 is completely powered down. When the $\overline{CS}$ pin is toggled high-to-low, all internal circuitry starts to power up where it can take as long as 5µs for the TS7001's internal circuitry to power up completely. As a result, any conversion start sequence should not be initiated during this initial 5µs power-up delay.

Figure 9 shows a general operating diagram of the TS7001 in PM Mode 1. The analog input signal is sampled on the second low-to-high SCLK transition following the initial high-to-low $\overline{CS}$ transition. System timing design should incorporate a 5-µs delay between the high-to-low $\overline{CS}$ transition and the second low-to-high SCLK transition. In microcontroller applications, this is achieved by

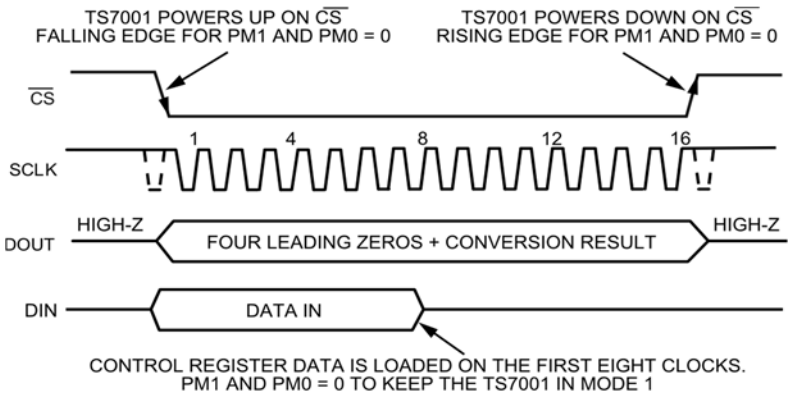


Figure 9: TS7001's Power Management Mode 1 Operation Diagram.

driving the $\overline{CS}$ pin from one of the host processor's port lines and ensuring that the serial data read (from the microcontroller's serial port) is not initiated for at least 5µs.

In DSP applications, where the $\overline{CS}$ signal is derived typically from the DSP's serial frame synchronization port, it is usually not possible to separate a high-to-low $\overline{CS}$ transition and a second low-to-high SCLK transition by up to 5µs without affecting the DSP system serial clock speed. Therefore, system timing design should incorporate a WRITE to the TS7001's control register to terminate PM Mode 1 operation and program the ADC into PM Mode 2; that is, by writing [PM1,PM0] = [0,1] into the TS7001's control register. To get a valid conversion result, a second conversion must be initiated when the ADC is powered up. A WRITE operation that takes place with this second conversion can program the ADC back into PM Mode 1 where the power-down operation is enabled when the $\overline{CS}$ pin is toggled high

Power Management Mode 2 Operation: [PM1,PM0] = [0,1]

Regardless of the status of the $\overline{CS}$ signal, the TS7001 remains fully powered up in this mode of operation. PM Mode 2 should be used for fastest throughput rate performance because the system timing design does not need to incorporate the TS7001's 5-µs power-up delay time. Figure 10 shows the general operating diagram for the TS7001 in PM Mode 2.

Serial data programmed into the TS7001 at the DIN input during the first eight clock cycles of data transfer are loaded to the control register. For the TS7001 to remain in PM Mode 2, system timing design must always write [PM1, PM0] = [0,1] into the control register on every serial input data transfer.

A high-to-low $\overline{CS}$ transition initiates the conversion sequence and the analog input signal is sampled on the second low-to-high SCLK transition. Sixteen serial clock cycles are required to complete the conversion and to transfer the conversion result to the host processor. Another conversion can be initiated immediately by toggling the $\overline{CS}$ pin low again once data transfer is complete (that is, once the $\overline{CS}$ signal is toggled high).

Power Management Mode 3 Operation: [PM1, PM0] = [1,0]

In this mode, the TS7001 is automatically powered down at the end of every conversion. It is similar to PM Mode 1 except that the status of the $\overline{CS}$ signal in PM Mode 3 does not have any effect on the power-down status of the TS7001.

Figure 11 shows the general operating diagram of the TS7001 in PM Mode 3. On the first high-to-low SCLK transition after $\overline{CS}$ is toggled low, all TS7001's internal circuitry starts to power up. Similarly to PM Mode 1, it can take as long as 5µs for the TS7001's internal circuitry to power up completely. As a result, any conversion start sequence should not be initiated during this initial 5-µs power-up delay. The analog input signal is sampled on the second low-to-high SCLK transition following the high-to-low $\overline{CS}$ transition. As shown in Figure 18, system timing design should incorporate a 5-µs delay between the first high-to-low $\overline{SCLK}$ transition and the second low-to-high SCLK transition after the high-to-low $\overline{CS}$ transition.

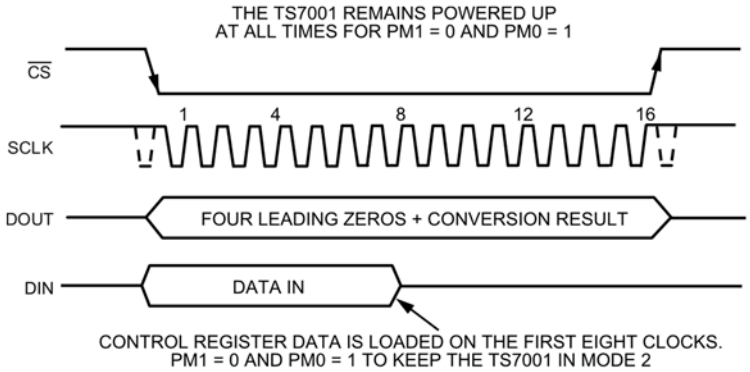


Figure 10: TS7001's Power Management Mode 2 Operation Diagram.

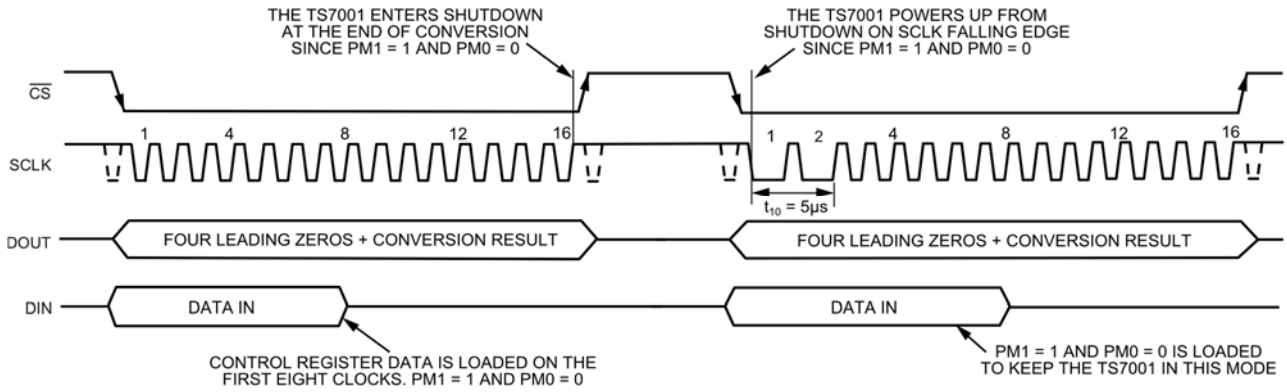


Figure 11: TS7001's Power Management Mode 3 Operation Diagram for Slow-SCLK Microcontrollers.

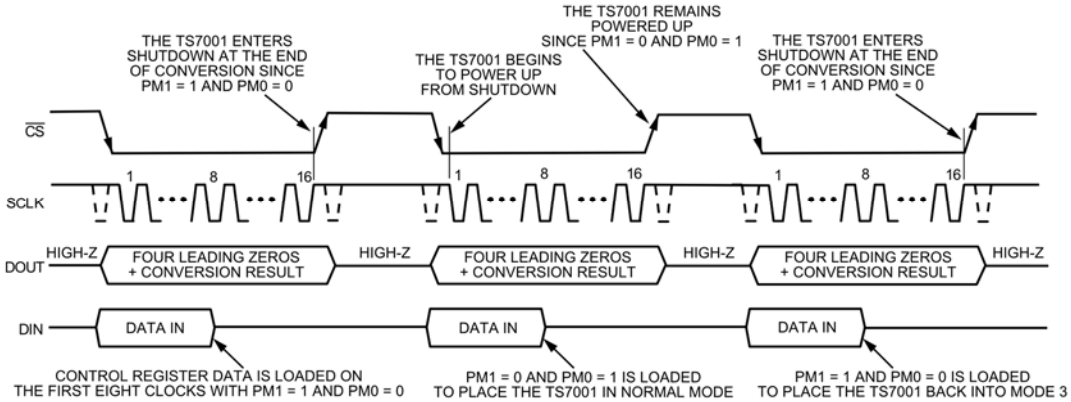


Figure 12: TS7001's Power Management Mode 3 Operation Diagram for Fast-SCLK Microcontrollers and DSPs.

In microcontroller applications (or in systems with a slow serial clock), the system timing design can be devised to accommodate this timing alignment by assigning the $\overline{CS}$ signal to one of the port lines and then adjusting the timing such that the serial data read (from the microcontroller's serial port) is not initiated for at least 5µs.

However, in systems with higher speed serial clocks (not unlike high-speed serial-clock DSP applications), it may not be possible to insert a 5µs delay between ADC power up and the first low-to-high SCLK transition. Therefore, system timing design should incorporate a WRITE to the TS7001's control register to terminate the ADC's PM Mode 3 operation and program the TS7001 into PM Mode 2; that is, by writing [PM1,PM0] = [0,1] into the TS7001's control register. To get a valid conversion result, a second conversion must be initiated when the ADC is powered up – see Figure 19. A WRITE operation that takes place with this second conversion can program the ADC back into PM Mode 3 where the power-down operation is enabled when the conversion sequence terminates.

Power Management Mode 4 Operation: [PM1,PM0] = [1,1]

In PM Mode 4, the TS7001 is automatically placed in standby (or sleep) mode at the end of every conversion. In this mode, all internal circuitry is powered down except for the internal 2.5-V reference. PM Mode 4 is similar to PM Mode 3; in this case, the power-up delay time is much shorter (1µs vs 5µs) because the internal reference remains powered up at all times.

Figure 13 shows the general operating diagram of the TS7001 in PM Mode 4. On the first high-to-low SCLK transition after the $\overline{CS}$ pin is toggled low, the TS7001 is powered up out of its standby mode. Since the TS7001's power-up delay time PM Mode 4 is very short, powering up the ADC and executing a conversion with valid results in the same read/write operation is feasible. The analog input signal is

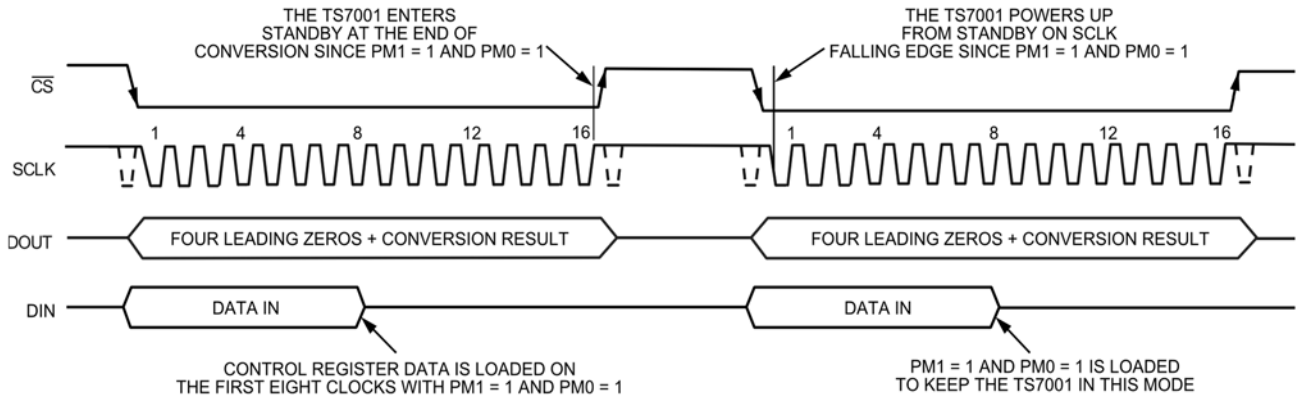


Figure 13: TS7001's Power Management Mode 4 Operation Diagram.

sampled on the second low-to-high SCLK transition following the high-to-low $\overline{CS}$ transition. At the end of conversion (after the last low-to-high SCLK transition), the ADC is powered down automatically back into its standby mode.

The TS7001's Serial Interface Description

Figure 14 shows the detailed timing diagram for TS7001's serial interface. The serial clock provides the conversion clock and also controls the transfer of data to/from the TS7001 during conversion.

The $\overline{CS}$ signal initiates the serial data transfer and controls the TS7001's conversion process. In PM Modes 1, 3, and 4, a high-to-low $\overline{CS}$ transition powers up the ADC. In all cases, the $\overline{CS}$ signal gates SCLK to the TS7001 and sets the ADC's internal track-and-hold into track mode. The analog input signal is then sampled on the second low-to-high SCLK transition following the high-to-low $\overline{CS}$ transition. Thus, the analog input signal is acquired during the first 1.5 SCLK clock cycles (t_{ACQ}) after the high-to-low $\overline{CS}$ transition. In modes where the high-to-low $\overline{CS}$ transition powers up the ADC, the acquisition time must include a 5-µs power-up delay. The ADC's internal track-and-hold moves from track mode to hold mode on the second low-to-high SCLK transition and a conversion is also initiated on this transition. The conversion process takes an additional 14.5 SCLK cycles to complete. After the conversion is completed, a subsequent low-to-high $\overline{CS}$ transition sets the serial data bus back into a high-Z (or three-state) condition. A new conversion can be initiated if the $\overline{CS}$ signal is left low.

In dual-channel operation, the current conversion result is associated to the selected analog channel programmed during the previous write cycle to the control register. Therefore, in dual-channel operation, the system code design must perform a channel address write for the next conversion while the current conversion is in progress.

Writing serial data to the Control Register always takes place and occurs on the first eight low-to-high

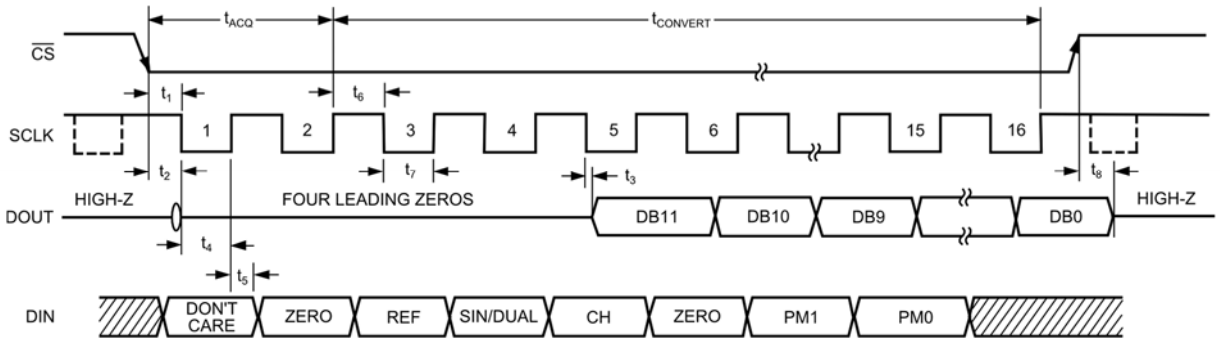


Figure 14: TS7001's Detailed Serial Interface Timing Diagram.

SCLK transitions. However, the TS7001 can be configured as a read-only device by physically loading all “zeros” (“0”s) into the Control Register every time, by applying a logic LOW to the DIN pin at all times, or by hard-wiring the DIN pin to GND. When the TS7001 is configured in WRITE/READ modes, system code design must be designed always to load the correct data onto the DIN line when reading data from the TS7001.

Sixteen serial clock cycles are required to perform the conversion process and to transfer data to/access data from the TS7001. In applications where the first serial clock transition following a high-to-low $\overline{CS}$ transition is a high-to-low SCLK transition, DOUT transitions from a high-Z state to a first leading zero; thus, the first low-to-high SCLK transition generates the first leading zero on DOUT. In applications where the first serial clock transition following a high-to-low $\overline{CS}$ transition is a low-to-high SCLK transition, the first leading zero may not be set up in time for the host processor to read it correctly. However, subsequent DOUT bits are transferred out on high-to-low SCLK transitions so that they are ready for the host processor on the following low-to-high SCLK transition. Thus, the second leading zero is transferred out on the high-to-low SCLK transition subsequent to the first low-to-high SCLK transition. Therefore, DOUT’s final bit in the data transfer is valid on the 16th low-to-high SCLK transition, having been transferred out of the ADC on the previous high-to-low SCLK transition.

Interfacing the TS7001 to Industry-Standard Microprocessors and DSPs

The serial interface on the TS7001 allows the ADC to be directly connected to a number of many microprocessors and DSPs. How to interface the TS7001 with some of the more common microcontroller and DSP serial interface protocols is covered in this section.

A TS7001 to TMS320C5x DSP Interface

With peripheral serial devices like the TS7001, the TMS320C5x’s serial interface has a continuous serial clock and frame synchronization signals to time the data transfer operations. A single logic inverter is the only glue logic required between the TMS320C5x’s CLKX output and the TS7001 SCLK input and is illustrated in the connection diagram of Figure 15. The TMS320C5x’s serial port is configured to operate in burst mode using the TMS320C5x’s internal CLKX (serial clock transmit)

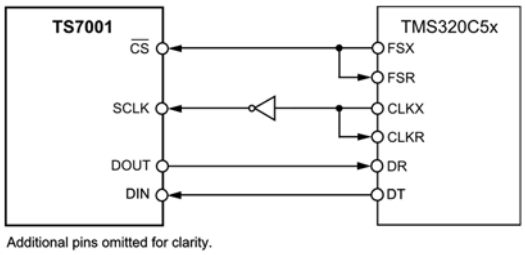


Figure 15: Interfacing the TS7001 to TMS320C5x-type DSPs.

and FSX (frame sync transmit) programmed as the TS7001’s $\overline{CS}$ input. The TMS320C5x’s serial port control register (SPC) must be configured in the following manner:

Table 3: TMS320C5x Serial Port Control Register Setup

FO	FSM	MCM	TXM
0	1	1	1

A TS7001 to ADSP-21xx DSP Interface

The TS7001 is easily interfaced to the ADSP-21xx (or equivalent) family of DSPs using an inverter between the ADSP-21xx’s serial clock and the TS7001 as shown in Figure 16. The ADSP-21xx’s SPORT control register should be configured in Alternate Framing mode as shown in Table 4 and the ADSP-21xx’s serial clock frequency is set in its SCLKDIV register.

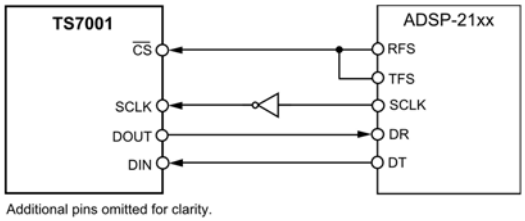


Figure 16: Interfacing the TS7001 to ADSP-21xx-type DSPs.

Table 4: SPORT0 Control Register Setup

Bit(s)	Setting	Description
TFSW, RFSW	1	Alternative framing
INVRFS, INVTFS	1	Active-low frame signal
DTYPE	00	Right justified data
SLEN	1111	16-bit data word
ISCLK	1111	Internal serial clock
TFSR, RFSR	1	Frame every word
IRFS	0	
ITFS	1	

With the ADSP-21xx's TFS and RFS pins of its SPORT connected together, the TFS is configured as an output and RFS configured as an input. The frame synchronization signal generated on the TFS output serves as the TS7001's $\overline{CS}$ input. In this example, however, since a timer interrupt is used to control the sampling rate of the ADC, it may not be possible to perform equidistant sampling (a required criterion in all signal processing applications) under certain application conditions.

The ADSP-21xx's timer registers are configured in such a manner that an interrupt is generated internally at the required sample interval. When the timer interrupt is received, an ADC control word is transmitted at the DT output with TFS. The TFS signal is then used to control the RFS and hence the data read from the TS7001. When the instruction to transmit with TFS is executed (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has toggled high-to-low-to-high before a transmission will commence. If the timer and SCLK values are set such that the instruction to transmit occurs on or near the low-to-high SCLK transition, data may be transmitted or the DSP may wait to transmit data until the next clock edge.

For example, consider an ADSP-2111 that has been chosen as the host processor. Since it has a 16-MHz master clock frequency, a SCLKDIV value of 3 is necessary to program its SPORT serial clock output to operate at 2MHz for the TS7001 (16MHz ÷ 2^3 = 2MHz); thus, eight master clock periods will elapse for every one TS7001 SCLK period. If the ADSP-2111's timer registers are loaded with a value of 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. Because the transmit instruction occurs on an SCLK edge, non-equidistant sampling is the result. The DSP will implement equidistant sampling only if the number of SCLKs between interrupts is a whole integer number.

A TS7001 to DSP56xxx DSP Interface

Connecting the TS7001 for use with Freescale's (nee Motorola's) DSP56xxx family of DSPs is shown in Figure 17 where an inverter is used between the DSP56xxx's SCK output and the TS7001's SCLK input. The DSP56xxx's SSI (synchronous serial interface) is configured in synchronous mode (SYN bit = 1 in CRB) with an internally generated 1-bit clock period frame sync for both Tx and Rx (Bits FSL1 = 1 and FSL0 = 0 in CRB). Word length is set to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA.

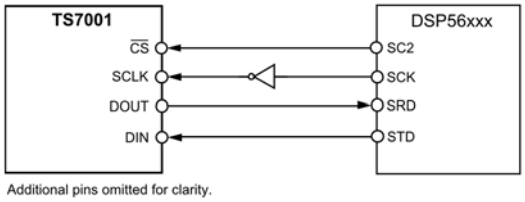


Figure 17: Interfacing the TS7001 to DSP56xxx-type DSPs.

A TS7001 to 68HC11 Microcontroller Interface

Connecting the TS7001 to Freescale's 68HC11 (nee Motorola's MC68HC11) is shown in Figure 18. The microcontroller's serial peripheral interface (SPI) is configured for Master Mode (MSTR = 1) with its Clock Polarity Bit (CPOL) set to 1 and Clock Phase Bit (CPHA) set to 1. Serial data transfer from the TS7001 to the 68HC11 requires two 8-bit transfers and the 68HC11's SPI is configured by writing to the SPI Control Register (SPCR) — consult the *68HC11 User Manual* for more information.

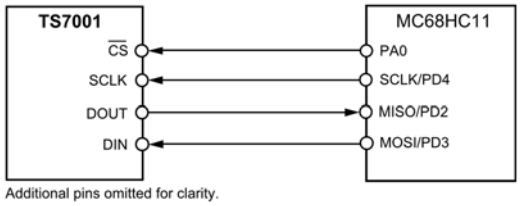


Figure 18: Interfacing the TS7001 to 68HC11-type Microcontrollers.

A TS7001 to 8051 Microcontroller Interface

Using the parallel port of legacy 8051-type (or equivalent) microcontrollers, a serial interface to the TS7001 can be designed as shown in Figure 19. As a result, full duplex serial transfer to be implemented. The technique involves "bit-banging" one of the the microcontroller's I/O ports (for

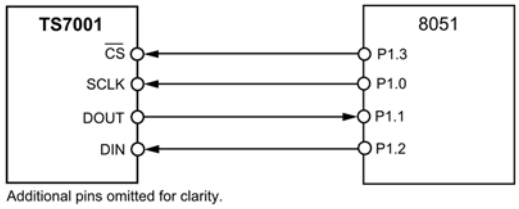


Figure 19: Interfacing the TS7001 to Legacy 8051-type Microcontrollers.

example, P1.0) to generate a serial clock and using two other I/O ports (for example, P1.1 for DOUT and P1.2 for DIN) to transfer data from/to the TS7001.

A TS7001 to PIC16C6x/PIC16C7x Microcontroller Interface

As shown in Figure 20, the connection between the TS7001 and the PIC16C6x/PIC16C7x is simple and does not require any glue logic circuits. The PIC16C6x synchronous serial port (SSP) is configured as an SPI master with its clock polarity bit set to 1 by writing to the synchronous serial port control register (SSPCON). In this example, I/O port RA1 is being used to generate the TS7001's $\overline{CS}$ signal. Since this microcontroller family only transfers eight bits of data during each serial transfer operation, two consecutive read/write operations are required. For additional information, please consult the *PIC16/PIC17 Microcontroller User Manual*.

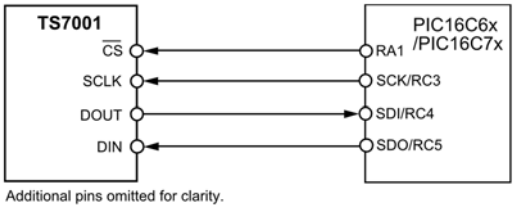


Figure 20: Interfacing the TS7001 to PIC16C6x/PIC16C7x-type Microcontrollers.

APPLICATIONS INFORMATION

Ground Plane Management and Layout

For best performance, printed circuit boards should always be used and wire-wrap boards are not recommended. Good PC board layout techniques ensure that digital and analog signal lines are kept separate from each other, analog and digital (especially clock) lines are not routed parallel to one another, and high-speed digital lines are not routed underneath the ADC package.

A contiguous analog ground plane should be routed under the TS7001 to avoid digital noise coupling. A single-point analog ground (star ground point) should be created at the ADC's GND and separate from any digital logic ground. All analog grounds as well as the ADC's GND pin should be connected to the star ground. No other digital system ground should be made to this ground connection. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

Even though the TS7001's exhibits excellent supply rejection as shown in th Typical Operating Characteristics, it is always considered good engineering practice to prevent high-frequency noise on the TS7001's VDD power supply from affecting the ADC's high-speed comparator. Therefore, the VDD supply pin should be bypassed to the star ground with 0.1µF and 10µF capacitors in parallel and placed close to the ADC's Pin 2 as was shown in Figure 4. Component lead lengths should be very short for optimal supply-noise rejection. If the power supply is very noisy, an optional 10-Ω resistor inserted in series with the TS7001's VDD pin can be used in conjunction with the bypass capacitors to form a low-pass filter.

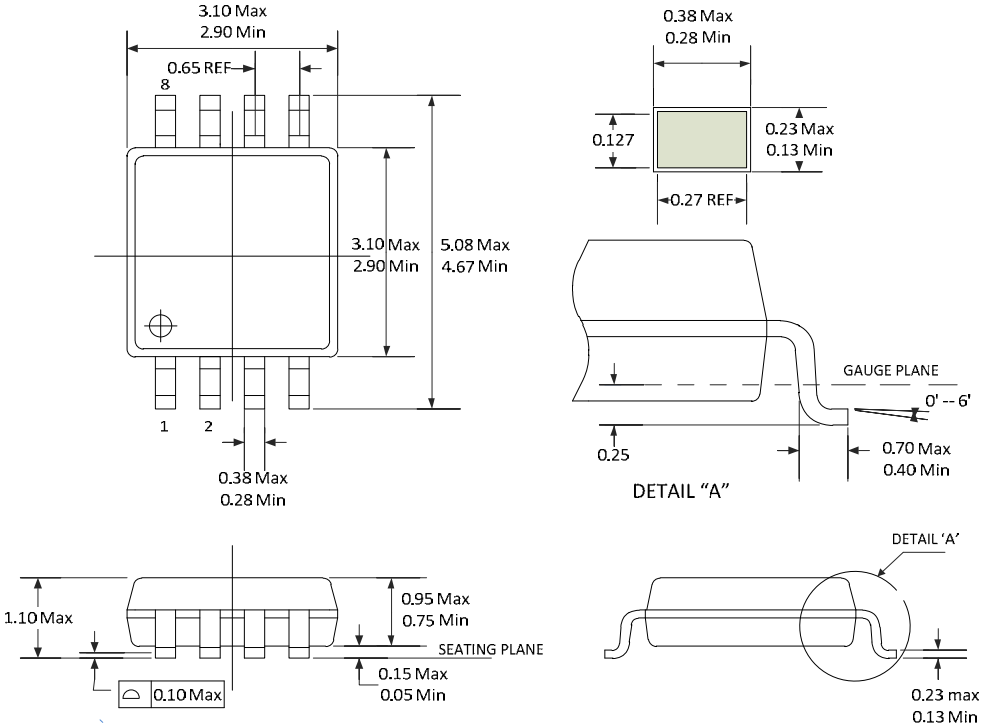
Evaluating the TS7001's Dynamic Performance

The recommended layout for the TS7001 is outlined in the demo board manual for the TS7001. The demo board kit includes a fully assembled/tested demo board and documentation describing how to evaluate the TS7001's dynamic performance using Silicon Labs proprietary TSDA-VB data acquisition/capture kit.

PACKAGE OUTLINE DRAWING

8-Pin MSOP Package Outline Drawing

(N.B., Drawings are not to scale)



NOTE:

1. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
2. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTUSIONS.
3. CONTROLLING DIMENSION IN MILIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC MO-187 VARIATIONS AA
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.

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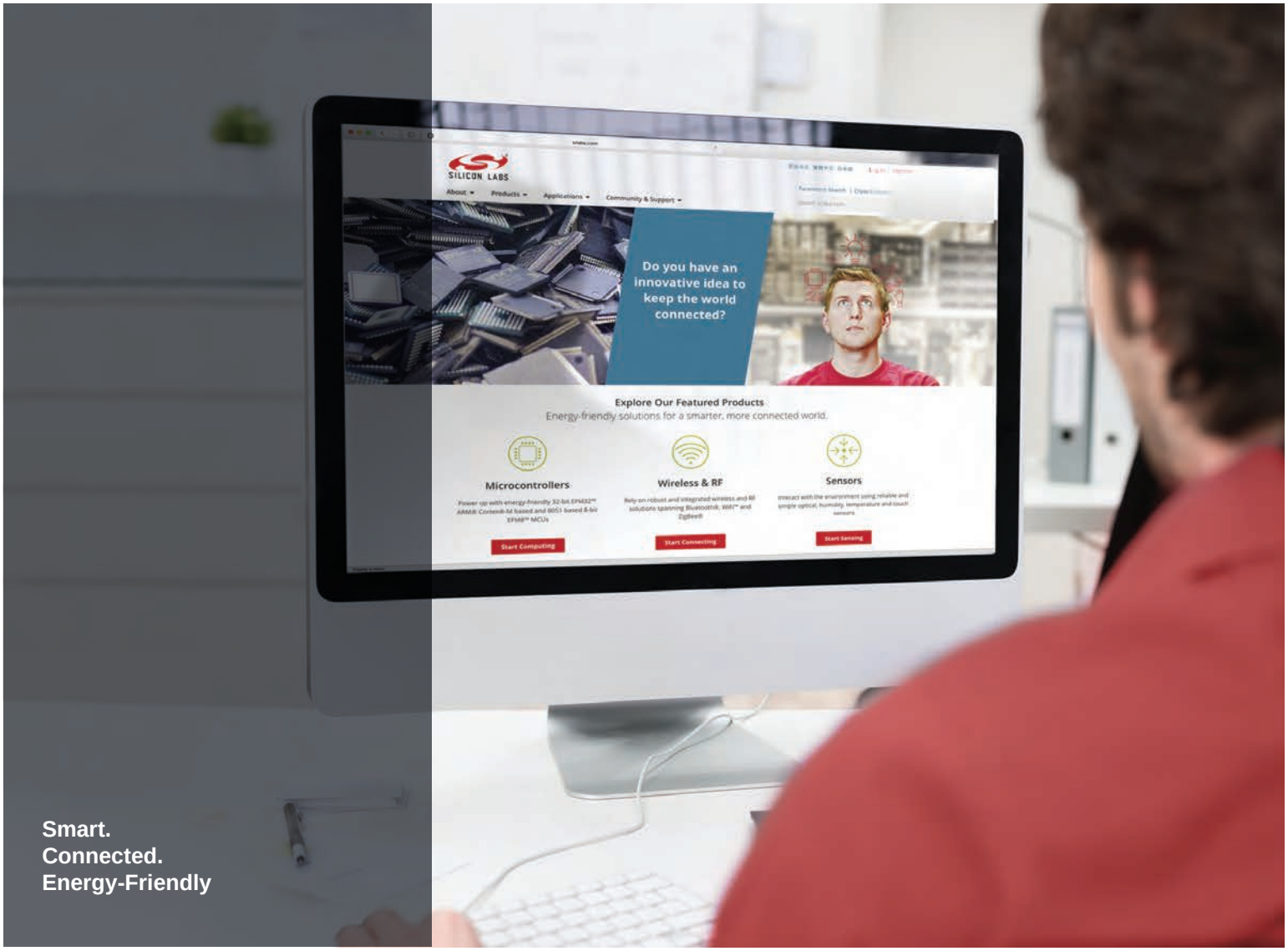

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